Claim 36, line 1, change "36" to --34--.

Please rewrite claims 1, 2, 4, 5, 7, 30, and 33 in amended form as follows:

1. (Amended) A bus system, comprising:

(a) a plurality of bus elements;

(b) a central unit having a plurality of bus inputs and an output, with the central unit coupling at least one of the inputs to the output;

(c) a first plurality of uni-directional point-to-point buses [coupling] for coupling in a first predetermined direction the bus elements to the central unit bus inputs;

(d) a second plurality of uni-directional point-to-point buses [coupling] for coupling in a second predetermined direction the output of the central unit to each of the bus elements; and

(e) arbitration logic connected to the plurality of bus inputs of the central unit to which the first plurality of uni-directional point-to-point buses connect, the arbitration logic for granting the bus elements access through the central unit one at a time based upon requests from the bus elements.

2. (Amended) A system as recited in claim 1, wherein the system further includes a first state device that is disposed at the output of the central unit, the state device for controlling the output of the central unit.

4. (Amended) A system as recited in claim 2, wherein the central unit includes a multiplexer for multiplexing the bus inputs from the first plurality of uni-directional point-to-point buses.

5. (Amended) A system as recited in claim 4, wherein the system further includes a second state device at each input to the central unit, with the second state devices also being connected to the arbitration logic.

7. (Amended) A system as recited in claim 6, wherein the arbitration logic includes a scheduler and an arbiter, with the scheduler and arbiter being connected.

30. (Amended) A system comprising:

a plurality of central processing units;

a shared memory;

a central unit including:

combining logic for accepting a plurality of inputs at least equal to the number of the central processing units plus memory and coupling at least one of inputs to its output;

arbitration logic for controlling which of the inputs is provided at the output;

a memory controller providing a memory input to the combining logic and receiving a memory output from the combining logic;

a plurality of first uni-directional point-to-point buses, with one bus coupling each of the central processing units to an input of the combining logic, and with each of the first uni-directional point-to-point buses for coupling in a first predetermined direction a central processing unit to an input of the combining logic;

a first uni-directional memory bus [coupling] for coupling in a second predetermined direction the memory to the memory controller;

a plurality of second uni-directional point-to-point buses [coupling] for coupling in a third predetermined direction the output of the combining logic to the central processing units; and

a second uni-directional memory bus [coupling] for coupling in a fourth predetermined direction the output of the memory to the memory control logic.

33. (Amended) A method of implementing a high speed bus to which a plurality of bus elements are coupled comprising the steps of:

(a) coupling with a first uni-directional bus in a first predetermined direction each of the bus elements to a central unit [with a separate first uni-directional bus having a direction from the bus elements to the central unit];

(b) selecting with arbitration means one of the first bus inputs to the central unit to be an output; and

(c) coupling with a second uni-directional bus in a second predetermined direction said output to each of the bus elements [over a second uni-directional bus having a direction from the central unit to the bus elements].

Please add new claims 37-40 as follows:

~~37~~ 9. The bus system as recited in claim 2, wherein the first state device includes a latch.

~~38~~ 8. The bus system as recited in claim 5, wherein the each of the second state devices includes a latch.

~~39~~ 32. The bus system as recited in claim 1, wherein a bus element includes a CPU.